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Applicant: Toshiba Corporation

DE

Specification

1. Title of the Invention

Display Controller

2. Claims

1. A display controller, characterized in that an LSI chip for performing display control for controlling a display apparatus to display a character, an image or the like has built therein at least part of an image memory for storing information for displaying a character, an image or the like and a display control circuit for reading out display data from said image memory.

2. The display controller according to claim 1, characterized in that said display controller includes no interface with said image memory in connection between said LSI chip and the outside.

3. The display controller according to claim 1, characterized in that a memory having a plurality of input/output ports is used as said image memory.

3. Detailed Description of the Invention

[Object of the Invention]

(Technical Field to which the Invention Pertains)

This invention relates to a display controller for use with a computer apparatus.

(Prior Art)

For a display apparatus for use with a computer apparatus, progressively high functions are required so that the display apparatus may serve as the core of the man-machine interface. Multi-color display, image display, multi-window display and so forth are representative ones of such functions, and in order to implement any of the functions, a high speed response is required for a display controller and a display memory.

Conventionally, in order to cause a display apparatus to display a character, a graphic form or the like, a display controller and an image memory are connected to each other, and the display controller performs readout control of the image memory. The display controller has evolutionally changed from a display controller of a board level assembled from various parts to another display controller in the form of an LSI. However, in a display system, an access performance to the image memory, an interface bus width for the display controller and so forth have been significant necks to performances.

(Problem to be Solved by the Invention)

As described above, the performances of a display subsystem are conventionally determined by the memory performances such as the access time of an external

memory. Further, the number of connection pins of the display controller and the image memory cannot be increased because of formation of the display controller as an LSI or in terms of the cost, and also it is a problem that the bus width of the memory makes a neck to the performances.

In recent years, the degree of integration of an LSI has increased gradually, and it has become possible for a chip to have even a memory of a large capacity in the inside thereof. Further, the memory in a chip has a significant merit that even a specific memory can be constructed without being restricted by the number of pins (memory bus width and so forth).

The present invention has been made in view of such circumstances as described above, and it is an object of the present invention to provide a display controller wherein an image memory is provided in a chip so that miniaturization and improvement in performance can be achieved.

[Constitution of the Invention]

(Means for Solving the Problem)

According to the present invention, a display controller is characterized in that an LSI chip for displaying for controlling a display apparatus to display

a character, an image or the like has built therein at least part of an image memory for storing information for displaying a character, an image or the like and a display control circuit for reading out data for display from the image memory.

(Operation)

According to the present invention, as described hereinabove, an image memory (or a character font memory) for retaining information for being displayed on a display apparatus and a display controller for generating a synchronizing signal, a blanking signal and so forth necessary for the display apparatus to display and performing display control for displaying data stored in the image memory on the display apparatus. Consequently, a memory interface signal is unnecessary and miniaturization can be anticipated. Further, by forming the internal image memory in a suitable structure, high speed processing responding to a memory access is implemented.

Further, since the image memory is provided in the inside of the chip, the bus width of the image memory can be increased without being restricted by the number of pins. Further, since contention of memory accesses can be prevented by forming the memory as a multi-port memory,

higher speed memory accessing can be anticipated.

(Embodiments)

In the following, embodiments of the present invention are described with reference to the drawings. FIG. 1 is a block diagram showing an embodiment of the present invention. Referring to FIG. 1, reference numeral 19 denotes a display controller chip of a one-chip configuration which has built therein an image memory and a display control circuit for reading out display data from the image memory and performing display output control. The display controller chip 19 is formed from functional components denoted by reference numerals 11 to 13 and 15 to 17 and accesses the built-in memory to perform display of a graphic form, a character or the like. Reference numeral 11 denotes a display control circuit, which performs production of a synchronizing signal, a blanking signal and so forth to the display apparatus 14 and performs control for reading out data from an image memory 12 and displaying the data. Reference numeral 12 denotes an image memory which stores information necessary for display. Reference numeral 13 denotes a display output circuit, which converts data read out from the image memory 12 into serial data (a video signal) and supplies the serial data to the

external display apparatus 14. Reference numeral 14 denotes a display apparatus, which displays a character, a graphic form or the like in accordance with a video signal outputted from the display output circuit 13 of the display controller chip 19. Reference numeral 15 denotes a memory data bus, which is used for data transfer of the image memory 12. Reference numeral 16 denotes a transfer plotting circuit, which performs transfer, plotting of a graphic form or the like of a region designated from within image memory data. Reference numeral 17 denotes a system interface control circuit, which controls transfer of data to and from the outside. Reference numeral 18 denotes a system data bus, by which external data is connected to the display controller chip 19.

FIGS. 2 and 3 are block diagrams showing different embodiments of the present invention.

FIG. 2 is a block diagram showing an embodiment wherein text display is performed. Referring to FIG. 2, reference numeral 21 denotes a display control circuit, which performs production of a synchronizing signal, a blanking signal and so forth to a display apparatus and performs control of reading out data from an image memory 22 and displaying the data. Reference numeral 22 denotes

an image memory, which stores information of a character code or the like. Reference numeral 23 denotes a font memory, which stores font images corresponding to character codes. Reference numeral 24 denotes a display output circuit, which converts data read out from the font memory 23 into serial data and supplies the video signal to an external display apparatus. Reference numeral 25 denotes a system interface control circuit, which controls data transfer from and to the outside.

FIG. 3 is a block diagram of an embodiment wherein an image memory built in a display controller chip is formed as a multi-port image memory. Referring to FIG. 3, reference numeral 31 denotes a display control circuit, which performs production of a synchronizing signal, a blanking signal and so forth to a display apparatus and performs control of reading out data from an image memory 32 and displaying the data. Reference numeral 32 denotes an image memory having two ports, and the image memory 32 stores information necessary for display. Reference numeral 33 denotes a display output circuit, which converts data read out from the image memory 32 into serial data and supplies the video signal to the external display apparatus. Reference numeral 34 denotes a transfer plotting circuit, which performs transfer,

plotting of a graphic form or the like of a region designated from within image memory data. Reference numeral 35 denotes a system interface control circuit, which controls data transfer to and from the outside. Reference numeral 36 denotes a display readout address, and a display address from the display control circuit 31 is supplied to the image memory 32. Reference numeral 37 denotes an image memory address, and an address when memory accessing other than display memory accessing is to be performed is supplied. Reference numeral 38 denotes a display data bus, and data read out from the address 36 is supplied through this bus to the display output circuit 33. Reference numeral 39 denotes a memory data bus, which uses the address 37 to perform data transfer to and from the image memory 32.

In the following, operation of the embodiments of the present invention is described in detail. First, description is given of the embodiment shown in FIG. 1. The display control circuit 11 reads out contents of the image memory 12, and the display data is converted from parallel data into serial data by the display output circuit 13 to produce video data conforming to the external display apparatus 14 and the video data is outputted. Further, the display control circuit 11

accesses the image memory 12 in order to perform, in addition to the display operation, transfer (BIT-BLT: Bit-boundary Block Transfer) of a designated rectangular region or plotting or filling of a graphic form such as a straight line or a circle by means of the transfer plotting circuit 16 and so forth. Further, from the outside, accessing to the image memory 12 is performed by the system interface control circuit 17.

Since the image memory 12 is included in the chip (display controller chip 19), the bus width of the memory data bus 15 can be made greater than that where it is externally provided, and the performance can be raised. In the display controller chip 19, the external interface can be formed only from the system interface control circuit 18 and a video interface connecting to the display apparatus 14, and miniaturization can be anticipated.

FIG. 2 shows an embodiment wherein text display is performed. Only a display operation by the display circuit different from that of FIG. 1 is described. The display control circuit 21 reads out a code and data of an attribute or the like from the image memory 22 and reads out an image from the font memory 23 in accordance with the code, and the image is converted into a video

signal by the display output circuit 24.

FIG. 3 shows an embodiment wherein the image memory shown in FIG. 1 is modified into a two-port memory. Upon reading out for display from the image memory 32, an address is supplied from the display control circuit 31 to the image memory 32 through the address bus 36, and data read out from the 2-port image memory 32 is transmitted from the data bus 38 to the display output circuit 33 and converted into a video output by the display output circuit 33. Image memory accessing other than that for display is performed by the address bus 37 and data bus 39 different from each other. In this manner, since the image memory 32 has a plurality of buses including an address bus and a data bus different from each other, it has a characteristic that it allows independent accessing thereto and higher speed operation can be anticipated.

[Effects of the Invention]

As described above, according to the present invention, an LSI chip for displaying for controlling a display apparatus to display a character, an image or the like has built therein at least part of an image memory for storing information for displaying a character, an image or the like and a display control circuit for

reading out display data from the image memory. Consequently, a memory interface to the image memory becomes unnecessary and miniaturization can be anticipated. Further, since the memory can be provided in the inside of the chip, the bus width of the memory can be increased. Further, where the memory is formed as a multi-port memory, contention of memory accesses can be prevented and higher speed memory accessing can be anticipated.

4. Brief Description of the Drawings

FIG. 1 is a block diagram showing an embodiment of the present invention, and FIGS. 2 and 3 are block diagrams individually showing different embodiments of the present invention.

11 … display control circuit, 12 … image memory, 13 … display output circuit, 14 … display apparatus, 15 … memory data bus, 16 … transfer plotting circuit, 17 … system interface control circuit, 18 … system data bus, 19 … display controller chip, 22 … image memory, 23 … font memory, 32 … 2-port image memory.

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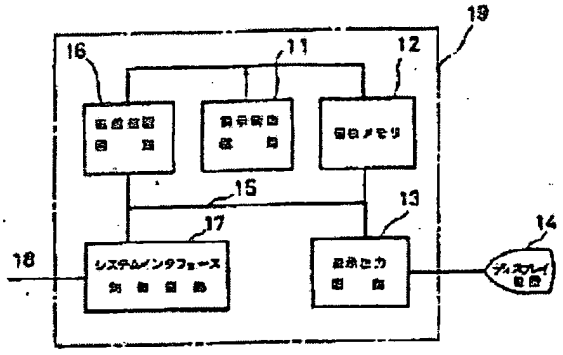
FIG. 1



第 1 図

11: display control circuit

12: image memory

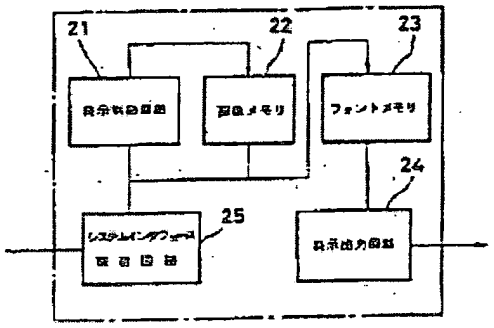
13: display output circuit

14: display apparatus

16: transfer plotting circuit

17: system interface control circuit

FIG. 2



第 2 図

21: display control circuit

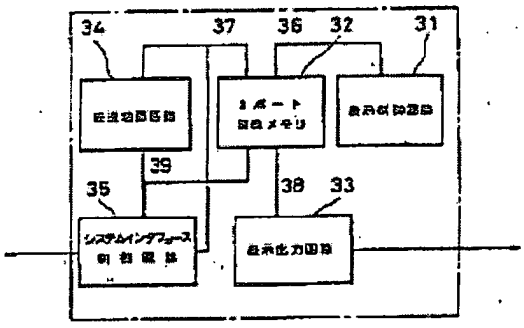
22: image memory

23: font memory

24: display output circuit

25: system interface control circuit

FIG. 3



第 3 図

31: display control circuit

32: 2-port image memory

33: display output circuit

34: transfer plotting circuit

35: system interface control circuit